1 38	L Number	Hits	Search Text	DB	Time stamp
2 2139 interconnect\$3 adj3 information.			(soft adj macro) and ((hard adj macro) or		2003/06/03 12:59
2 2139 interconnect\$3 adj3 information					
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Section Sect				_	0000/00/00
Section	2	2139	interconnect\$3 adj3 information	•	2003/06/03 13:00
DERWENT; IBM TDB USPAT; US-POPUB; EPO; JPO; DERWENT; IBM TDB USPAT; US-POPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; U	1				
3 5274 Optimiz\$3 adj4 design					
3 5274 Optimiz\$3 adj4 design		1	·	· ·	
US-PGPUB; EPO; JPO; DERMENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; JPO; DERMENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; JPO; JPO; JPO; JPO; JPO; JPO; J	1,	5274	ontimiz\$3 adi4 design		2003/06/03 13:01
274323 Optimiz\$3 Optimiz	3	52/4	opermizes and design .	•	2003,00,03 13.01
DERMENT; IBM TOB USPAT;			*		
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274323 optimiz\$3 Optimiz\$3 USPAT; US					
Second S	4	274323	optimiz\$3		2003/06/03 13:01
1000 design\$3 adj3 integrated adj3 circuit EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT	-				
11000 design\$3 adj3 integrated adj3 circuit IBM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT; U			·		
1000 design\$3 adj3 integrated adj3 circuit USPĀT; US-PCPUB; EPO; JPO; DERWENT; IBM_TDB USPĀT; US-PCPUB; EP					
10911 bandwidth and latency US-PGPUB; EPO, JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO, JPO; DERWENT; US-PGPUB; EPO, JPO; DERWENT; US-PGPUB; EPO, JPO; DERWENT; US-PGPUB; EPO,			·		
Bed 10911 bandwidth and latency	5	11000	design\$3 adj3 integrated adj3 circuit		2003/06/03 13:02
DERMENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DPO; EPO; DPO; EPO; DPO; EPO; DPO; EPO; DPO; EPO; EPO; DPO; EPO;				•	
10911 bandwidth and latency	-				
10911 bandwidth and latency		1		1	,
US-PGPUB EPO; JPO; DERMENT; IBM_TDB 2003/06/03 13: US-PGPUB EPO; JPO; JPO; DERMENT; IBM_TDB 2003/06/03 13: US-PGPUB EPO; JPO; JPO; JPO; JPO; JPO; JPO; JPO; J				_	2002/06/02 12:02
Record R	6	10911	pandwidth and latency	-	2003/06/03 13:03
DERMENT; IBM_TDB LOS-PAT; US-PGPUB; EPG; JPO; DERMENT; IBM_TDB US-PAT; US-PGPUB; EPG; JPO; JPO; DERMENT; IBM_TDB US-PAT; US-PGPUB; EP					
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development	7 .	9611	(design adi3 environment) or (design adi3		2003/06/03 13:04
8 390 (optimiz\$3 adj4 design) and (design\$3 adj3 IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; JPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; JPO; JPO; JPO; JPO; JPO; JPO; J	'	3611		1	
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Integrated adj3 circuit US-PGPUB; EPC; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; and (design adj3 environment) or (design adj3 US-PGPUB; and (design\$\frac{3}{3}\) adj3 integrated adj3 circuit) US-PGPUB; EPC; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; and (design\$\frac{3}{3}\) adj4 design) US-PGPUB; EPC; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; and (design\$\frac{3}{3}\) adj3 integrated adj3 US-PGPUB; EPC; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPC; JPO; JPO; USPAT; US-PGPUB; US	100		•		
Integrated adj3 circuit) US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM	8	390	(optimiz\$3 adj4 design) and (design\$3 adj3	USPAT;	2003/06/03 13:04
107 ((design adj3 environment) or (design adj3 USPĀT; USPGPUB; EPO; JPO; DERWENT; IBM TDB USPĀT; USPĀT; USPGPUB; EPO; JPO; DERWENT; IBM TDB USPĀT; USPĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀTĀT					
107 ((design adj3 environment) or (design adj3 development)) and ((optimiz\$3 adj4 design) and (design\$3 adj3 integrated adj3 circuit)) Libm_TDB Li	1	1			
107 ((design adj3 environment) or (design adj3 development)) and ((optimiz\$3 adj4 design) and (design\$3 adj3 integrated adj3 circuit)) EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DER				· ·	
development) and ((optimiz\$3 adj4 design) and (design\$3 adj3 integrated adj3 circuit))					2002/05/02 12 51
and (design\$3 adj3 integrated adj3 circuit)) EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; and (design\$3 adj3 integrated adj3 USPAT; US-PGPUB; and (bandwidth and latency) USPAT; USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; USPAT; US-PGPU	9	107			2003/06/03 13:04
DERWENT; IBM_TDB Continuent		1	development)) and ((optimiz\$3 adj4 design)		
10 (((design adj3 environment) or (design adj3 development)) and ((optimiz\$3 adj4 design) and (design\$3 adj3 integrated adj3 circuit))) and (bandwidth and latency) 11 127 (interconnect\$3 adj3 information) and (bandwidth and latency) 12 3 (optimiz\$3 adj4 design) and ((interconnect\$3 adj3 information) and (bandwidth and latency)) 13 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 15 26 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 16 27 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 17 (design\$3 adj4 design)) 18 2003/06/03 13: 19 2003/06/03 13: 2003/06/03 13: 2003/06/03 13: 2003/06/03 13:			and (designs adja integrated adja circuit))		
10					· 0.
development)) and ((optimiz\$3 adj4 design) and (design\$3 adj3 integrated adj3 circuit))) and (bandwidth and latency) 11 127 (interconnect\$3 adj3 information) and (bandwidth and latency) 12	10		[[[design adi3 environment] or [design adi3]		2003/06/03 13:05
and (design\$3 adj3 integrated adj3 circuit))) and (bandwidth and latency) 127 (interconnect\$3 adj3 information) and (bandwidth and latency) 128 (optimiz\$3 adj4 design) and ((interconnect\$3 adj3 information) and (bandwidth and latency)) 139 (optimiz\$3 adj4 design) and ((interconnect\$3 adj3 information) and (bandwidth and latency)) 140 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 150 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 150 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 150 (optimiz\$3 adj4 design) 160 (optimiz\$3 adj4 design) 170 (optimiz\$3 adj4 design) 180 (optimiz\$3 adj4 design) 190 (optimiz\$3 adj4 design)	10		development)) and ((ontimiz\$3 adi4 design)		2505,00,05 15.05
circuit)) and (bandwidth and latency) (interconnect\$3 adj3 information) and (bandwidth and latency) (bandwidth and latency) (optimiz\$3 adj4 design) and ((interconnect\$3 adj3 information) and (bandwidth and latency)) (optimiz\$3 adj4 design) (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) (optimiz\$3 adj4 design) (interconnect\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (spAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGP		-	and (design\$3 adi3 integrated adi3		
11 127 (interconnect\$3 adj3 information) and (bandwidth and latency) 12 3 (optimiz\$3 adj4 design) and ((interconnect\$3 adj3 information) and (bandwidth and latency)) 13 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design)) 18 24 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design)) 19 2003/06/03 13: 10 2003/06/03 13: 2003/06/03 13: 2003/06/03 13: 2003/06/03 13: 2003/06/03 13: 2003/06/03 13: 2003/06/03 13:					
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(bandwidth and latency) (bandwidth and latency) (bandwidth and latency) (coptimiz\$3 adj4 design) and ((interconnect\$3 adj3 information) and (bandwidth and latency)) (coptimiz\$3 adj4 design) (coptimiz\$3 adj4 design) (coptimiz\$3 adj4 design) (coptimiz\$3 adj3 integrated adj3 circuit) and (coptimiz\$3 adj4 design)	11	127	(interconnect\$3 adj3 information) and		2003/06/03 13:05
12 3 (optimiz\$3 adj4 design) and ((interconnect\$3 uspat; latency)) 13 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design) 15 26 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 16 27 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (optimiz\$3 adj4 design))		1		US-PGPUB;	
12 3 (optimiz\$3 adj4 design) and ((interconnect\$3 uSPAT; uS-PGPUB; EPO; JPO; DERWENT; IBM_TDB uSPAT; (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design) 15 26 (design\$3 adj3 integrated adj3 circuit) and ((interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design)) 16 27 (design\$3 adj3 integrated adj3 circuit) and (coptimiz\$3 adj4 design)) 17 28 (design\$3 adj3 integrated adj3 circuit) and (coptimiz\$3 adj4 design))					
3 (optimiz\$3 adj4 design) and ((interconnect\$3 USPAT; adj3 information) and (bandwidth and latency)) 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 46 (design\$3 adj4 design) 47 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 48 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 49 (design\$3 adj4 design)	. 8		*		
adj3 information) and (bandwidth and latency)) 13 US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; US-PGPUB; IBM_TDB USPAT; US-PGPUB; EPO; JPO; US-PGPUB; EPO; JPO; US-PGPUB; EPO; JPO; US-PGPUB; EPO; JPO;					
latency)) 13 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design)) 25 EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; (optimiz\$3 adj4 design)) 26 COO3/06/03 13:	12	3			2003/06/03 13:07
13 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 15 DERWENT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) 16 DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;					
13 45 (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design) 14 24 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (coptimiz\$3 adj4 design) 18			latency))		
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(optimiz\$3 adj4 design) US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; ((interconnect\$3 adj3 integrated adj3 circuit) and ((optimiz\$3 adj4 design)) US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;	,,		(intermediate = 322 information) ind	-	2002/06/02 12:07
EPO; JPO; DERWENT; IBM_TDB (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;	13	45			2003/00/03 13:0/
14 24 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;			(opcimizs) adj4 design)		
14 24 (design\$3 adj3 integrated adj3 circuit) and (interconnect\$3 adj3 information) and (optimiz\$3 adj4 design)) IBM_TDB USPAT; 2003/06/03 13: US-PGPUB; EPO; JPO;			0		
14 24 (design\$3 adj3 integrated adj3 circuit) and USPAT; 2003/06/03 13: ((interconnect\$3 adj3 information) and USPAT; US-PGPUB; (optimiz\$3 adj4 design)) EPO; JPO;					
((interconnect\$3 adj3 information) and US-PGPUB; (optimiz\$3 adj4 design)) EPO; JPO;	14	24	(decion\$3 adi3 integrated adi3 circuit) and		2003/06/03 13:08
(optimiz\$3 adj4 design)) EPO; JPO;	17	24			-555,55,55
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IBM TDB			*	· ·	

-		5235	(optimiz\$3 adj4 integrate adj2 circuit) or	USPAT;	2003/06/03 07:28
			(optimiz\$3 adj3 design\$3)	US-PGPUB;	
				EPO; JPO;	
				DERWENT;	i l
			•	IBM TDB	
			16 manusements addit integrated addit	USPAT;	2003/06/02 14:54
-		0	self-programmable adj3 integrated adj2		· ' '
			circuit	US-PGPUB;	· •
				EPO; JPO;	
			· · · · · · · · · · · · · · · · · · ·	DERWENT;	·
				IBM_TDB	·
_		394	(design\$3 adj4 integrated adj circuit) and	USPAT;	2003/06/02 14:57
		1	((optimiz\$3 adj4 integrate adj2 circuit) or	US-PGPUB;	·
			(optimiz\$3 adj3 design\$3))	EPO; JPO;	
			(0)022245 aajs ass=54577	DERWENT;	
			*	IBM TDB	
		1	/1 = D	USPAT;	2003/06/02 14:57
-		0		•	2003/06/02 14:57
			circuit) and ((soft adj macro) and ((hard	US-PGPUB;	i
			adj macro) or (firm adj macro)))	EPO; JPO;	
				DERWENT;	
			• • •	IBM_TDB	
_		0	((design\$3 adj4 integrated adj circuit) and	USPAT;	2003/06/02 14:58
		1	((optimiz\$3 adj4 integrate adj2 circuit) or	US-PGPUB;	
	•	1	(optimiz\$3 adj3 design\$3))) and ((soft adj	EPO; JPO;	
.			macro) and ((hard adj macro) or (firm adj	DERWENT;	<i>;</i>
ľ			macro)))	IBM TDB	·
		_		_	2003/06/02 14:58
-		6	(design\$3 adj4 integrated adj circuit) and	USPAT;	2003/00/02 14:30
			((soft adj macro) and ((hard adj macro) or	US-PGPUB;	*
			(firm adj macro)))	EPO; JPO;	
				DERWENT;	
				IBM_TDB	
-		7	((optimiz\$3 adj4 integrate adj2 circuit) or	USPAT;	2003/06/02 15:04
			(optimiz\$3 adj3 design\$3)) and ((soft adj	US-PGPUB;	0.00
-			macro) and ((hard adj macro) or (firm adj	EPO; JPO;	
			macro)))	DERWENT;	
1				IBM TDB	
1.		8	self?programmable same integrated adj2	USPAT;	2003/06/02 15:37
- -	-	· •	circuit	US-PGPUB;	
			CIICUIC	EPO; JPO;	,
			· · · · · · · · · · · · · · · · · · ·	DERWENT;	. *
				IBM TDB	
			3	USPAT;	2003/06/02 15:16
-	•	12467	design\$3 adj4 integrated adj circuit		
À				US-PGPUB;	
			* '	EPO; JPO;	1
				DERWENT;	
		1			
-				IBM_TDB	0000/05/05 == ==
		38	(soft adj macro) and ((hard adj macro) or	USPAT;	2003/06/02 15:33
		38	(soft adj macro) and ((hard adj macro) or (firm adj macro))	USPAT; US-PGPUB;	2003/06/02 15:33
		38	(soft adj macro) and ((hard adj macro) or (firm adj macro))	USPAT;	2003/06/02 15:33
		38	(soft adj macro) and ((hard adj macro) or (firm adj macro))	USPAT; US-PGPUB;	2003/06/02 15:33
	· ·	38	(soft adj macro) and ((hard adj macro) or (firm adj macro))	USPAT; US-PGPUB; EPO; JPO;	2003/06/02 15:33
		*	(firm adj macro))	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/06/02 15:33
-		*	(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	_
_		*	(firm adj macro))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB;	_
_		*	(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;	_
_		*	(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT;	_
-		19	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro)))</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/02 15:34
-	:	*	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	_
-		19	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB;	2003/06/02 15:34
-		19	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT; US-PGPUB; EPO; JPO;	2003/06/02 15:34
-		19	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/06/02 15:34
		19	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/02 15:34
-		19	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2003/06/02 15:34
-		0	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/02 15:34
-		0	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2003/06/02 15:34
-		0	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB;	2003/06/02 15:34
		0	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/06/02 15:34
-		0	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and self?programmable</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/02 15:34
		0	optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and self?programmable (design\$3 adj4 integrated adj circuit) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT;	2003/06/02 15:34 2003/06/02 15:38 2003/06/02 15:38
-		0	<pre>(firm adj macro)) optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and self?programmable</pre>	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISM_TDB USPAT; US-PGPUB;	2003/06/02 15:34 2003/06/02 15:38 2003/06/02 15:38
-		0	optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and self?programmable (design\$3 adj4 integrated adj circuit) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;	2003/06/02 15:34 2003/06/02 15:38 2003/06/02 15:38
-		0	optimiz\$3 and ((soft adj macro) and ((hard adj macro) or (firm adj macro))) ((design\$3 adj4 integrated adj circuit) and ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3))) and self?programmable ((optimiz\$3 adj4 integrate adj2 circuit) or (optimiz\$3 adj3 design\$3)) and self?programmable (design\$3 adj4 integrated adj circuit) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISM_TDB USPAT; US-PGPUB;	2003/06/02 15:34 2003/06/02 15:38 2003/06/02 15:38

-	2447	self?programmable	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2003/06/02 15:39
-	2447		EPO; JPO;	
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-		design adj3 environment	USPAT;	2003/06/03 07:45
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	274323	optimiz\$3	USPAT;	2003/06/03 07:30
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	660	(design adj3 environment) and optimiz\$3	USPAT;	2003/06/03 .07:30
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			EPO; JPO;	
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	172	macro and ((design adj3 environment) and	USPAT;	2003/06/03 07:30
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		optimiz\$3)	US-PGPUB;	
			EPO; JPO;	
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			IBM_TDB	
-	111	hard and (macro and ((design adj3	USPAT;	2003/06/03 07:30
		environment) and optimiz\$3))	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
_	47	soft and (hard and (macro and ((design adj3	USPAT;	2003/06/03 07:31
		environment) and optimiz\$3)))	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
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	1080	design adj environment	USPAT;	2003/06/03 07:49
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-	54		USPAT;	2003/06/03 07:47
	*	(firm adj macro))	US-PGPUB;	
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	1.	macro) and ((hard adj macro) or (firm adj	US-PGPUB;	
		macro)))	EPO; JPO;	
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-	28	(design adj environment) same optimiz\$3	USPAT;	2003/06/03 07:49
	20	(design da) environment, same optimizes	US-PGPUB;	
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